CLAIMS

What is claimed is:

[Note: Square bracketed **bold** *and italicized* **cross-referencing text** is provided in the below claims as an aid for readability and for finding corresponding (but not limiting) support in the specification. The square-bracketed text is not intended to add any limitation whatsoever to the claims and should be deleted in all legal interpretations of the claims and should also be deleted from the final published version of the claims.]

1. A field programmable gate array (FPGA) device **[*100,1000*]** comprising:

(a) a first plurality P1 of repeated logic units **[*VGBs,102,1021*]** wherein:

(a.1) each said logic unit is user-configurable to acquire and process at least a second plurality P2 of input logic bits **[*Fig.6A*]** and to responsively produce result data having at least a third plurality P3 of output logic bits **[*Fig.6B*]**,

(a.2) said logic units are distributed among a plurality of horizontal rows, with each row of the plurality of rows having a fourth plurality P4 of said logic units;

(b) a fifth plurality P5 of horizontal interconnect channels (HIC's) [*150*] correspondingly distributed adjacent to said horizontal rows of logic units, wherein:

(b.1) each said horizontal interconnect channel (HIC) includes at least P3 interconnect lines, and

(b.2) each said horizontal row of P4 logic units is configurably couplable to at least a corresponding one of the P6 HIC's at least for acquiring input logic bits from the corresponding HIC or at least for outputting result data to the corresponding HIC; and

(c) an embedded memory subsystem [*114/116*], wherein said embedded memory subsystem includes:

(c.1) a sixth plurality P6 of memory blocks [ML0-MR7], and wherein:

(c.1a) each said memory block is embedded within one of said rows of logic units [*102*] and is configurably couplable to the corresponding HIC of said row for transferring storage data by way of the corresponding HIC of that row of P4 logic units; and

(c.1b) each of said memory blocks includes at least a first address-capturing register

[*1011*] that is programmably couplable [*1062,1064*] to at least one of said HIC's [*1050*] for receiving and capturing an address signal [*1051,1052*] supplied on said at least one HIC.

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2. A FPGA device [*100*] according to Claim 1 wherein:

(a.3) said logic units are further distributed among a plurality of vertical columns, with each column of the plurality of columns having a seventh plurality P7 of said logic units; and

(c.1b) plural ones of said memory blocks are arranged to define one or more columns [*114/116*] of embedded memory within said device [*100*] with each such column having an eighth plurality P8 of said memory blocks.

3. A field programmable gate array device [*100*] according to Claim 2 wherein:

(c.1c) each said memory block is organized as a ninth plurality P9 of addressable sets of storage data bits, where each addressable set of storage data bits includes at least P3 bits, said P3

number corresponding to the P3 number of output logic bits producible by each said logic unit.

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4. A field programmable gate array device [*100*] according to Claim 3 wherein:

(c.1c1) each of P2 and P3 is an integer equal to or greater than 4.

5. A field programmable gate array device [*100*] according to Claim 1 wherein:

(a.3) groups of said logic units are further wedged together such that each group of logic units defines a logic superstructure [*101,440*]; and

(c.1c) groups of said memory blocks [*470,480*] are also wedged together such that each group of memory blocks defines a memory superstructure that is configurably-couplable to a corresponding logic superstructure [*440*].

6. A field programmable gate array device [*100*] according to Claim 1 wherein said embedded memory subsystem includes:

(c.2) at least one special interconnect channel [*466*] for supplying address signals to the first address-capturing registers [*1011*] of a respective set of said memory blocks.

7. A field programmable gate array device [*100*] according to Claim 6 wherein:

(c.1b1) there are at least two of said columns [*114/116*] of embedded memory; and

(c.2a) there are at least two of said special interconnect channels [*164,166*], and each respective special interconnect channel is for supplying address signals to a respective one of the at least two columns of embedded memory.

8. A field programmable gate array device [*100*] according to Claim 6 wherein:

(c.1c) each said memory block has at least first and second data ports [*884,882*] each for outputting storage data;

(c.1d) each said memory block has at least first and second address ports [*874,872*] each for receiving address signals identifying the storage data to be

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output by a corresponding one of the at least first and second data ports;

(c.1e) each said memory block has in addition to said respective first address-capturing register, a second address-capturing register [*1012*] that is programmably couplable [*1062,106C*] to at least one of said HIC's [*1050*] for receiving and capturing an address signal [*1051,1052*] supplied on said at least one HIC, and said first and second address-capturing registers respectively service the first and second address ports; and

(c.2a) the at least one special interconnect channel includes first and second address-carrying components [*862a,862b*] along which independent address signals may be respectively carried for application to respective ones of the first and second address ports [*874,872*] of at least two memory blocks.

9. A field programmable gate array device [*100*] according to Claim 1 wherein:

(c.1d) each said memory block has a controls-receiving port [*873*] for programmably

acquiring control signals that control operations of said memory block; and

(c.1e) each respective first address-capturing register [*1011*] is clocked by a respective first address clock signal [*ADRCLK1,1015*] acquired by said controls-receiving port.

10. In a field programmable gate array device (FPGA) [*100*] having a user-configurable interconnect network that includes a plurality of horizontal interconnect channels [*150*] each with a diversified set of long-haul interconnect lines [*MaxL*] and shorter-haul interconnect lines [*2xL-8xL*], an embedded memory subsystem [*114/116*] comprising:

(a) a plurality of multi-ported memory blocks [*ML0-MR7*] each arranged adjacent to a horizontal interconnect channel (HIC) [*850*] of the interconnect network;

wherein:

(a.1) each multi-ported memory block [*870*] includes a first, independently-addressable data port [*884*] and a second, independently-addressable data port [*882*];

(a.2) each of said first and second, independently-addressable data ports includes a respective address-capturing register [*1011,1012*] that is connected by user-

configurable intercouplings [*855*] to one or both of the long-haul interconnect lines [*859*] and the shorter-haul interconnect lines [*852-858*] for capturing a respective address signal [*1051,1052*].

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11. In an FPGA device having a plurality of variable grain, configurable logic blocks (VGB's) [*102*] and interconnect resources including lines of diversified continuous lengths [*2xL-8xL,MaxL*] for interconnecting said VGB's, an embedded memory subsystem comprising:

a plurality of memory blocks [*470,480*] wherein each memory block includes:

(a) at least a first address-capturing register [*1011*] that is programmably couplable [*1062,1064*] to said interconnect resources [*1050*] for receiving and capturing a respective first address signal [*1051,1052*] supplied by way of said interconnect resources.

12. The embedded memory subsystem of Claim 11 wherein each memory block further includes:

(b) a second address-capturing register [*1012*] that is programmably couplable [*1062,1064*] to said interconnect resources [*1050*] for receiving and capturing a respective second address signal [*1051,1052*] supplied by way of said interconnect resources.

13. The embedded memory subsystem of Claim 11 wherein:

(a.1) said first address-capturing register [*1011*] is further programmably couplable [*1065*] to said interconnect resources [*1057*] for receiving a respective first address clock signal [*ADRCLK1,1015*] to which the first address-capturing register is responsive.

14. A method [*Fig.10*] for use in an FPGA device having plural variable grain blocks (VGB's) [*102*], diversified interconnect resources, and an embedded memory subsystem comprising a plurality of memory blocks [*870*] situated for configurable coupling to the diversified interconnect resources, where the memory blocks each have at least one address input port [*872,874*] and at least one data port [*882,884*], the address input port having a respective address-capturing register [*1011*], said method comprising the steps of:

(a) outputting [*1023,1031*] a first address signal for conveyance by at least part of said interconnect resources [*1051,1052*] to an address input port of a given memory block;

(b) capturing the conveyed first address signal in the respective address-capturing register [*1011*] of the given memory block; and

(a) while the first address signal is captured, outputting [*1027,1032*] a next address signal for conveyance by at least part of said interconnect resources to the address input port of the given memory block.

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15. The method of Claim 14 wherein said step (a) of outputting the first address signal includes the substep of:

(a.1) transmitting the first address signal through a configurable sequential output element [*CSEQ,1023*] of a first of said VGB's.

16. The method of Claim 15 wherein said step (a) of outputting the first address signal includes the further substep of:

(a.2) sourcing the first address signal from a storage register [*1022*] within a configurable sequential element [*CSE*] of said first of said VGB's.

17. The method of Claim 16 wherein said step (a) of outputting the first address signal includes the further substep of:

(a.3) applying an address-changing clock signal [*1022a*] to the storage register that sources the first address signal, where said address-changing clock signal is derived from an address-validating clock

signal [*1057,1015*] applied to the address-capturing register [*1011*].

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18. The method of Claim 14 wherein said step (a) of outputting the first address signal includes the substeps of:

(a.1) transmitting the first address signal through a first of plural tristate drivers [*1031,1032*], where each of the tristate drivers has an output enabling terminal [*1035,1036*];

(a.2) providing an address-changing control signal [*1043*] that deactivates the output enabling terminal [*1035*] of the first tristate driver, where said address-changing control signal is derived from an address-validating clock signal [*1057,1015*] applied to the address-capturing register [*1011*].

19. A method [*Fig.10*] for configuring an FPGA device having plural variable grain blocks (VGB's) [*102*], configurable interconnect resources, and an embedded memory subsystem comprising one or more memory blocks [*870*] situated for configurable coupling via the configurable interconnect resources to the VGB's, where the memory blocks each have at least one registered address input port [*872*] for receiving and storing supplied address bits, said method comprising the steps of:

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(a) defining a first route [*1025,1062,1064*] through said interconnect resources from an address signal sourcing circuit [*1023,1031*] of the FPGA device to the at least one registered address input port [*872*]; and

(b) defining a second route [*1057,1067,1065*] through said interconnect resources from an address clock sourcing circuit [*1055*] of the FPGA device to the at least one registered address input port.

20. The FPGA configuring method [*Fig.10*] of Claim 19 further comprising the steps of:

(c) defining a third route [*1001*] through said interconnect resources from the address clock sourcing circuit [*1055*] to an address-changing circuit [*1021,1040*] of the FPGA device, the third route being configured such that a new address signal can be produced by action of said address-changing circuit substantially at the same time or shortly after an address clock signal [*1015*] of the address clock sourcing circuit [*1055*] clocks the at least one registered address input port, said new address signal being produced so as to not interfere with a current address signal [*1024,1034*] captured by the registered address input port.

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21. A method [*Fig.11B*] for producing configuration signals for configuring an FPGA device having plural variable grain blocks (VGB's) [*102*],

configurable interconnect resources, and an embedded memory subsystem comprising one or more memory blocks [*870*] situated for configurable coupling via the configurable interconnect resources to the VGB's, where the memory blocks each have at least one registered address input port [*872*] for receiving and storing supplied address bits, said method comprising the steps of:

(a) inputting [*1106*] a design definition;

(b) searching [*1107*] the input design definition for the presence of one or more memory modules [*1110*], address-sourcing modules [*1120*], and data-using modules [*1170*] that will cooperate to perform a memory read or memory write operation; and

(c) encouraging [*1108*] the creation in the configured FPGA of a shared signal route [*1160,1060*] that transmits an address-strobing clock signal [*1015*] to the registered address input port and transmits an address-change allowing signal [*1001*] to one or more of the address-sourcing modules [*1120,1023,1040*].